# MC10EP195, MC100EP195

# 3.3V ECL Programmable Delay Chip

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The MC10/100EP195 is a Programmable Delay Chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 3. The delay increment of the EP195 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 6 and Figure 4.

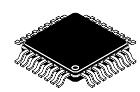
Because the EP195 is designed using a chain of multiplexers it has a fixed minimum delay of 2.2 ns. An additional pin D10 is provided for controlling Pins 14 and 15, CASCADE and $\overline{\text{CASCADE}}$, also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all “1” states on D[0:9] with SETMAX LOW to all “0” states on D[0:9] with SETMAX HIGH will increase the delay equivalent to “D0”, the minimum increment.

Select input pins D[10:0] may be threshold controlled by combinations of interconnects between $V_{EF}$ (pin 7) and $V_{CF}$ (pin 8) for LVCMOS, ECL, or LVTTL level signals. For LVCMOS input levels, leave $V_{CF}$ and $V_{EF}$ open. For ECL operation, short $V_{CF}$ and $V_{EF}$ (Pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to $V_{CF}$ and leave open $V_{EF}$ pin. The 1.5 V reference voltage to $V_{CF}$ pin can be accomplished by placing a 2.2 kΩ resistor between $V_{CF}$ and $V_{EE}$ for a 3.3 V power supply.

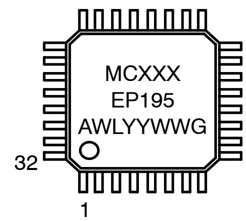
The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

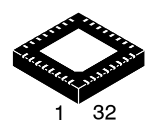
The 100 Series contains temperature compensation.

**MARKING DIAGRAM***

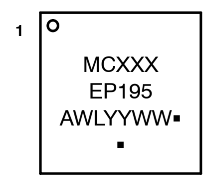


**LQFP−32**
**FA SUFFIX**
**CASE 873A**




**QFN32**
**MN SUFFIX**
**CASE 488AM**




| | | |
|---|---|---|
| XXX | = 10 or 100 |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

- Maximum Input Clock Frequency >1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.2 ns to 12.2 ns
- 10 ps Increments
- PECL Mode Operating Range:
  $V_{CC}$ = 3.0 V to 3.6 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the $\overline{\text{EN}}$ Pin Will Force Q to Logic Low
- D[10:0] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- $V_{BB}$ Output Reference Voltage
- Pb−Free Packages are Available

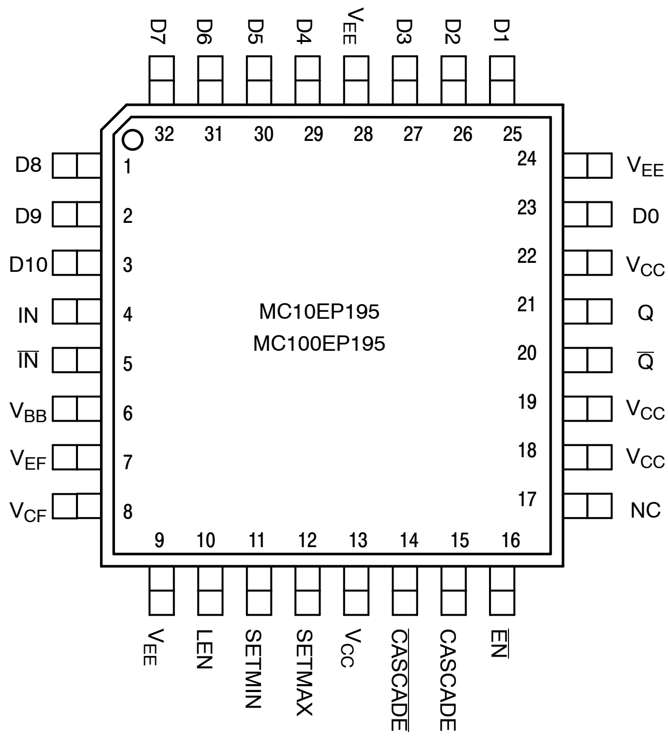



**Figure 1. 32−Lead LQFP Pinout** (Top View)

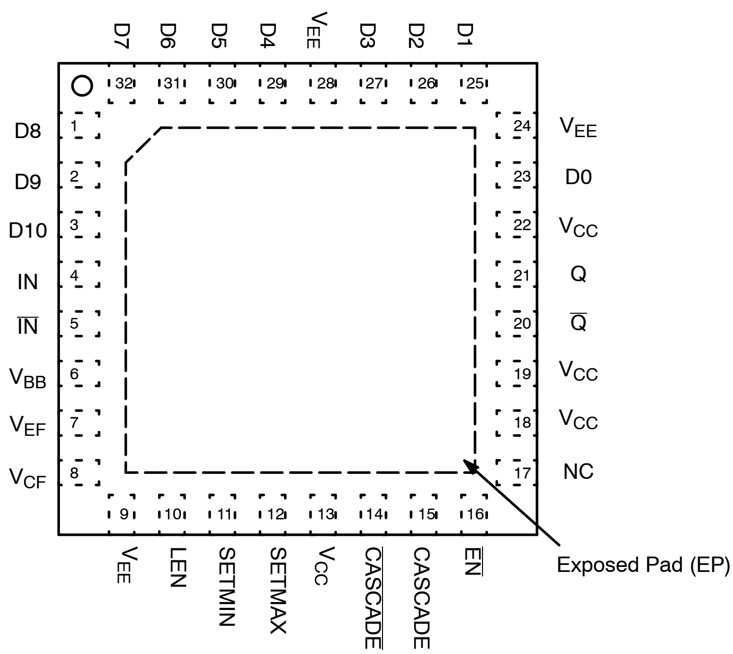



**Figure 2. 32−Lead QFN** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin | Name | I/O | Default State | Description |
|---|---|---|---|---|
| 23, 25, 26, 27, 29, 30, 31, 32, 1, 2 | D[0:9] | LVCMOS, LVTTL, ECL Input | Low | Single−Ended Parallel Data Inputs [0:9]. Internal 75 kΩ to $V_{EE}$. (Note 1) |
| 3 | D[10] | LVCMOS, LVTTL, ECL Input | Low | Single−Ended CASCADE/$\overline{\text{CASCADE}}$ Control Input. Internal 75 kΩ to $V_{EE}$. (Note 1) |
| 4 | IN | ECL Input | Low | Noninverted Differential Input. Internal 75 kΩ to $V_{EE}$. |
| 5 | $\overline{\text{IN}}$ | ECL Input | High | Inverted Differential Input. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| 6 | $V_{BB}$ | − | − | ECL Reference Voltage Output |
| 7 | $V_{EF}$ | − | − | Reference Voltage for ECL Mode Connection |
| 8 | $V_{CF}$ | − | − | LVCMOS, ECL, OR LVTTL Input Mode Select |
| 9, 24, 28 | $V_{EE}$ | − | − | Negative Supply Voltage. All $V_{EE}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 13, 18, 19, 22 | $V_{CC}$ | − | − | Positive Supply Voltage. All $V_{CC}$ Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 10 | LEN | ECL Input | Low | Single−ended D pins LOAD / HOLD input. Internal 75 kΩ to $V_{EE}$. |
| 11 | SETMIN | ECL Input | Low | Single−ended Minimum Delay Set Logic Input. Internal 75 kΩ to $V_{EE}$. (Note 1) |
| 12 | SETMAX | ECL Input | Low | Single−ended Maximum Delay Set Logic Input. Internal 75 kΩ to $V_{EE}$. (Note 1) |
| 14 | $\overline{\text{CASCADE}}$ | ECL Output | − | Inverted Differential Cascade Output for D[10]. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V. |
| 15 | CASCADE | ECL Output | − | Noninverted Differential Cascade Output. for D[10] Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V. |
| 16 | $\overline{\text{EN}}$ | ECL Input | Low | Single−ended Output Enable Pin. Internal 75 kΩ to $V_{EE}$. |
| 17 | NC | − | − | No Connect. The NC Pin is Electrically Connected to the Die and ”MUST BE” Left Open |
| 21 | Q | ECL Output | − | Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V. |
| 20 | $\overline{\text{Q}}$ | ECL Output | − | Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V. |

1. SETMIN will override SETMAX if both are high. SETMAX and SETMIN will override all D[0:10] inputs.
2. All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Table 2. CONTROL PIN**

| Pin | State | Function |
|---|---|---|
| EN | LOW (Note 3) | Input Signal is Propagated to the Output |
| | HIGH | Output Holds Logic Low State |
| LEN | LOW (Note 3) | Transparent or LOAD mode for real time delay values present on D[0:10]. |
| | HIGH | LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay. |
| SETMIN | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Minimum Output Delay |
| SETMAX | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Maximum Output Delay |
| D10 | LOW (Note 3) | CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH |
| | HIGH | $\overline{\text{CASCADE}}$ Output LOW, CASCADE Output HIGH |

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

**Table 3. CONTROL D[0:10] INTERFACE**

| | | |
|---|---|---|
| $V_{CF}$ | $V_{EF}$ Pin (Note 4) | ECL Mode |
| $V_{CF}$ | No Connect | LVCMOS Mode |
| $V_{CF}$ | 1.5 V ± 100 mV | LVTTL Mode (Note 5) |

4. Short $V_{CF}$ (pin 8) and $V_{EF}$ (pin 7).
5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, $R_{CF}$ (suggested resistor value is 2.2 kΩ ±5%), between $V_{CF}$ and $V_{EE}$ pins.

**Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE**

| POWER SUPPLY | CONTROL DATA SELECT INPUTS PINS (D [0:10]) | | | |
|---|---|---|---|---|
| | LVCMOS | LVTTL | LVPECL | LVNECL |
| PECL Mode Operating Range | YES | YES | YES | N/A |
| NECL Mode Operating Range | N/A | N/A | N/A | YES |

**Table 5. ATTRIBUTES**

| Characteristics | Value | |
|---|---|---|
| Internal Input Pulldown Resistor (R1) | 75 kΩ | |
| ESD Protection: Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 100 V<br>> 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 6) | Pb Pkg | Pb−Free Pkg |
| LQFP−32 | Level 2 | Level 2 |
| QFN−32 | − | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| Transistor Count | 1217 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

6. For additional information, see Application Note AND8003/D.

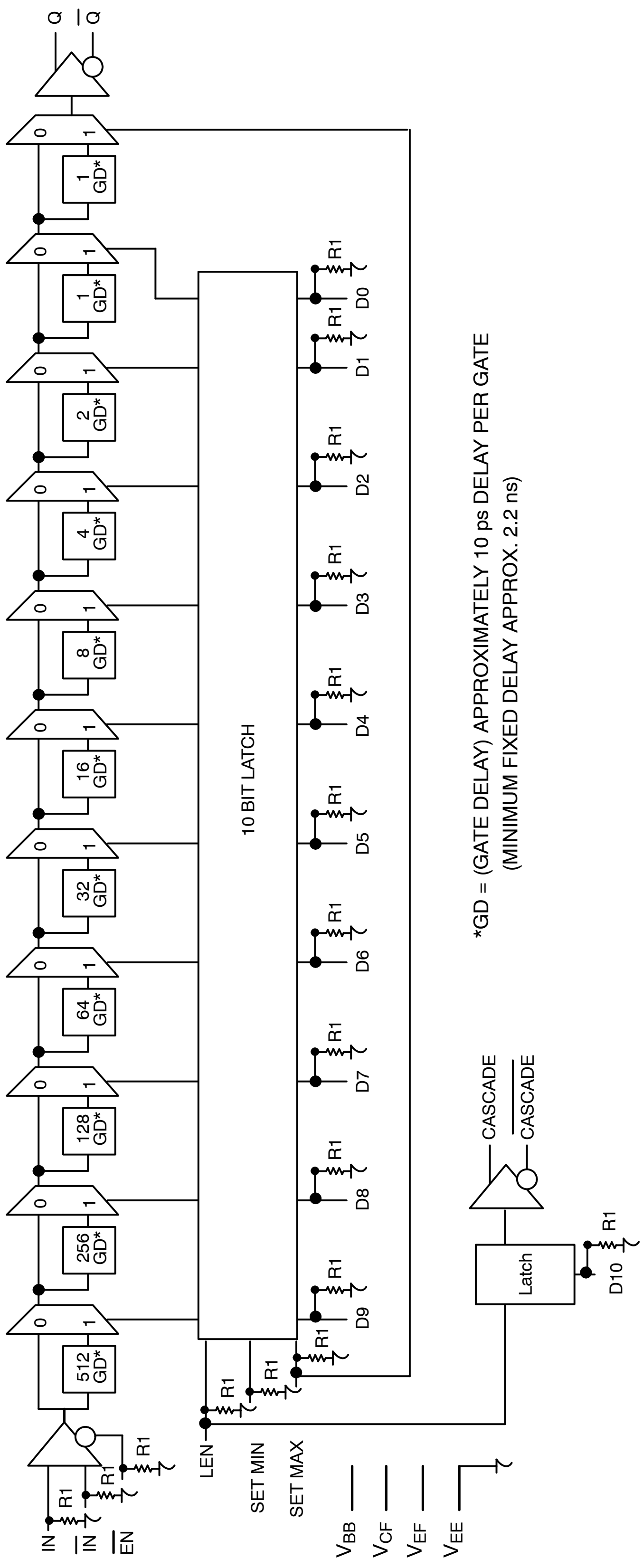



**Figure 3. Logic Diagram**

**Table 6. THEORETICAL DELAY VALUES**

| D(9:0) Value | SETMIN | SETMAX | Programmable Delay* |
|---|---|---|---|
| XXXXXXXXXX | H | L | 0 ps |
| 0000000000 | L | L | 0 ps |
| 0000000001 | L | L | 10 ps |
| 0000000010 | L | L | 20 ps |
| 0000000011 | L | L | 30 ps |
| 0000000100 | L | L | 40 ps |
| 0000000101 | L | L | 50 ps |
| 0000000110 | L | L | 60 ps |
| 0000000111 | L | L | 70 ps |
| 0000001000 | L | L | 80 ps |
| 0000010000 | L | L | 160 ps |
| 0000100000 | L | L | 320 ps |
| 0001000000 | L | L | 640 ps |
| 0010000000 | L | L | 1280 ps |
| 0100000000 | L | L | 2560 ps |
| 1000000000 | L | L | 5120 ps |
| 1111111111 | L | L | 10230 ps |
| XXXXXXXXXX | L | H | 10240 ps |

*Fixed minimum delay not included.

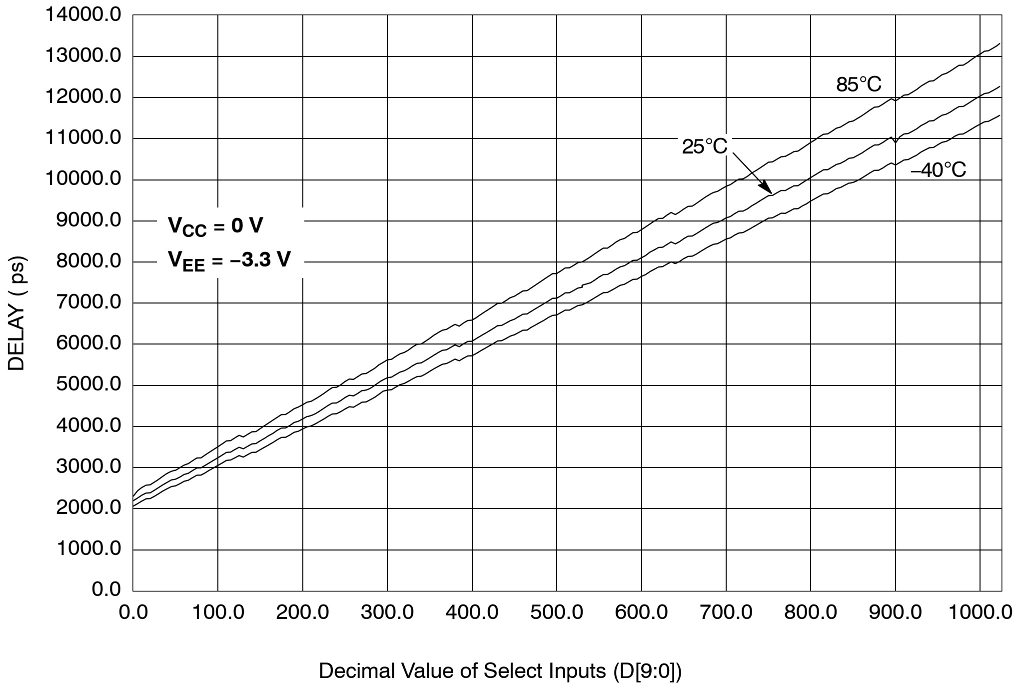



**Figure 4. Measured Delay vs. Select Inputs**

**Table 7. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | Negative Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | Positive Mode Input Voltage<br>Negative Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ±0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | LQFP−23<br>LQFP−23 | 80<br>55 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | LQFP−23 | 12 to 17 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | QFN−32<br>QFN−32 | 31<br>27 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P | QFN−32 | 12 | °C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C | | 265<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 8. 10EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 7)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 100 | 145 | 175 | 100 | 150 | 180 | 100 | 150 | 180 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 8) | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 8) | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended)<br>LVPECL<br>LVCMOS<br>LVTTL | <br>2090<br>2000<br>2000 | | <br>2415<br>3300<br>3300 | <br>2155<br>2000<br>2000 | | <br>2480<br>3300<br>3300 | <br>2215<br>2000<br>2000 | | <br>2540<br>3300<br>3300 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended)<br>LVPECL<br>LVCMOS<br>LVTTL | <br>1365<br>0<br>0 | | <br>1690<br>800<br>800 | <br>1430<br>0<br>0 | | <br>1755<br>800<br>800 | <br>1490<br>0<br>0 | | <br>1815<br>800<br>800 | mV |
| $V_{BB}$ | ECL Output Voltage Reference | 1790 | 1890 | 1990 | 1855 | 1955 | 2055 | 1915 | 2015 | 2115 | mV |
| $V_{CF}$ | LVTTL Mode Input Detect Voltage | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | V |
| $V_{EF}$ | Reference Voltage for ECL Mode Connection | 1900 | 2020 | 2150 | 1875 | 2080 | 2150 | 1850 | 2130 | 2150 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$)<br>IN<br>$\overline{IN}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −0.3 V.
8. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
9. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 9. 10EP DC CHARACTERISTICS, NECL** $V_{CC}$ = 0 V, $V_{EE}$ = −3.3 V to −3.0 V (Note 10)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 100 | 145 | 175 | 100 | 150 | 180 | 100 | 150 | 180 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 11) | −1135 | −1010 | −885 | −1070 | −945 | −820 | −1010 | −885 | −760 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 11) | −1935 | −1810 | −1685 | −1870 | −1745 | −1620 | −1810 | −1685 | −1560 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) LVNECL | −1210 | | −885 | −1145 | | −820 | −1085 | | −760 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) LVNECL | −1935 | | −1610 | −1870 | | −1545 | −1810 | | −1485 | mV |
| $V_{BB}$ | ECL Output Voltage Reference | −1510 | −1410 | −1310 | −1445 | −1345 | −1245 | −1385 | −1285 | −1185 | mV |
| $V_{EF}$ | Reference Voltage for ECL Mode Connection | −1400 | −1280 | −1250 | −1425 | −1220 | −1250 | −1450 | −1170 | −1250 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) IN / $\overline{IN}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with $V_{CC.}$ $V_{EE}$ can vary +0.3 V to −0.3 V.
11. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
12. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 10. 100EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 13)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 100 | 135 | 160 | 100 | 140 | 170 | 100 | 145 | 175 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 14) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 14) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended)<br>LVPECL<br>CMOS<br>TTL | <br>2075<br>2000<br>2000 | | <br>2420<br>3300<br>3300 | <br>2075<br>2000<br>2000 | | <br>2420<br>3300<br>3300 | <br>2075<br>2000<br>2000 | | <br>2420<br>3300<br>3300 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended)<br>LVPECL<br>CMOS<br>TTL | <br>1355<br>0<br>0 | | <br>1675<br>800<br>800 | <br>1490<br>0<br>0 | | <br>1675<br>800<br>800 | <br>1490<br>0<br>0 | | <br>1675<br>800<br>800 | mV |
| $V_{BB}$ | ECL Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{CF}$ | LVTTL Mode Input Detect Voltage | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | V |
| $V_{EF}$ | Reference Voltage for ECL Mode Connection | 1900 | 2020 | 2150 | 1875 | 2080 | 2150 | 1850 | 2130 | 2150 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$)<br>IN<br>$\overline{IN}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Input and output parameters vary 1:1 with $V_{CC.}$ $V_{EE}$ can vary +0.3 V to −0.3 V.
14. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
15. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC.}$ The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 11. 100EP DC CHARACTERISTICS, NECL** $V_{CC}$ = 0 V, $V_{EE}$ = −3.3 V (Note 16)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current (Note 17) | 100 | 135 | 160 | 100 | 140 | 170 | 100 | 145 | 175 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 18) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 18) | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) LVNECL | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) LVNECL | −1945 | | −1625 | −1945 | | −1625 | −1945 | | −1625 | mV |
| $V_{BB}$ | ECL Output Voltage Reference | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{EF}$ | Reference Voltage for ECL Mode Connection | −1400 | −1280 | −1250 | −1425 | −1220 | −1250 | −1450 | −1170 | −1250 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) IN<br>$\overline{IN}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

16. Input and output parameters vary 1:1 with $V_{CC.}$ $V_{EE}$ can vary +0.3 V to −0.3 V.
17. Required 500 lfpm air flow when using +5 V power supply. For ($V_{CC}$ − $V_{EE}$) > 3.3 V, 5 Ω to 10 Ω in line with $V_{EE}$ required for maximum thermal protection at elevated temperatures. Recommend $V_{CC}$ − $V_{EE}$ operation at ≤ 3.8 V.
18. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
19. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 12. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −3.0 V to −3.6 V or $V_{CC}$ = 3.0 V to 3.6 V; $V_{EE}$ = 0 V (Note 20)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Frequency | | 1.2 | | | 1.2 | | | 1.2 | | GHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay | | | | | | | | | | ps |
| | IN to Q; D(0−10) = 0 | 1650 | 2050 | 2450 | 1800 | 2200 | 2600 | 1950 | 2350 | 2750 | |
| | IN to Q; D(0−10) = 1023 | 9500 | 11500 | 13500 | 10000 | 12200 | 14000 | 10800 | 13300 | 15800 | |
| | $\overline{EN}$ to Q; D(0−10) = 0 | 1600 | 2150 | 2600 | 1800 | 2300 | 2800 | 2000 | 2500 | 3000 | |
| | D0 to CASCADE | 300 | 420 | 500 | 350 | 450 | 550 | 425 | 525 | 625 | |
| $t_{RANGE}$ | Programmable Range | | | | | | | | | | ps |
| | $t_{PD}$ (max) − $t_{PD}$ (min) | 7850 | 9450 | | 8200 | 10000 | | 8850 | 10950 | | |
| Δt | Step Delay (Note 21) | | | | | | | | | | ps |
| | D0 High | | 13 | | | 14 | | | | | |
| | D1 High | | 27 | | | 30 | | | | | |
| | D2 High | | 44 | | | 47 | | | 41 | | |
| | D3 High | | 90 | | | 97 | | | 100 | | |
| | D4 High | | 130 | | | 140 | | | 145 | | |
| | D5 High | | 312 | | | 335 | | | 360 | | |
| | D6 High | | 590 | | | 650 | | | 690 | | |
| | D7 High | | 1100 | | | 1180 | | | 1300 | | |
| | D8 High | | 2250 | | | 2400 | | | 2650 | | |
| | D9 High | | 4500 | | | 4800 | | | 5300 | | |
| mono | Monotonicity (Note 27) | | | | | TBD | | | | | |
| $t_{SKEW}$ | Duty Cycle Skew (Note 22) | | | | | | | | | | ps |
| | $\lvert t_{PHL} - t_{PLH} \rvert$ | | 25 | | | 25 | | | 25 | | |
| $t_s$ | Setup Time | | | | | | | | | | ps |
| | D to LEN | 200 | 0 | | 200 | 0 | | 200 | 0 | | |
| | D to IN (Note 23) | 300 | 140 | | 300 | 160 | | 300 | 180 | | |
| | $\overline{EN}$ to IN (Note 24) | 300 | 150 | | 300 | 170 | | 300 | 180 | | |
| $t_h$ | Hold Time | | | | | | | | | | ps |
| | LEN to D | 200 | 60 | | 200 | 100 | | 200 | 80 | | |
| | IN to $\overline{EN}$ (Note 25) | 400 | 250 | | 400 | 280 | | 400 | 300 | | |
| $t_R$ | Release Time | | | | | | | | | | ps |
| | $\overline{EN}$ to IN (Note 26) | 150 | −25 | | 150 | −75 | | 150 | −50 | | |
| | SET MAX to LEN | 400 | 200 | | 400 | 250 | | 400 | 300 | | |
| | SET MIN to LEN | 350 | 275 | | 350 | 200 | | 350 | 225 | | |
| $t_{jitter}$ | RMS Random Clock Jitter @ 1.2 GHz | | | | | | | | | | ps |
| | IN to Q; D(0:10) = 0 or SETMIN | | 0.86 | | | 1.16 | | | 1.12 | | |
| | IN to Q; D(0:10) = 1023 or SETMAX | | 0.89 | | | 1.09 | | | 1.02 | | |
| $V_{PP}$ | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Time @ 50 MHz | | | | | | | | | | ps |
| | 20−80% (Q) | 85 | 100 | 135 | 85 | 110 | 135 | 95 | 125 | 155 | |
| | 20−80% (CASCADE) | 100 | 140 | 200 | 110 | 150 | 200 | 130 | 170 | 220 | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

20. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
21. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
22. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
23. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
24. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
25. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
26. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
27. The monotonicity indicates the increasing delay value for each binary count increment on the control inputs D[9:0].

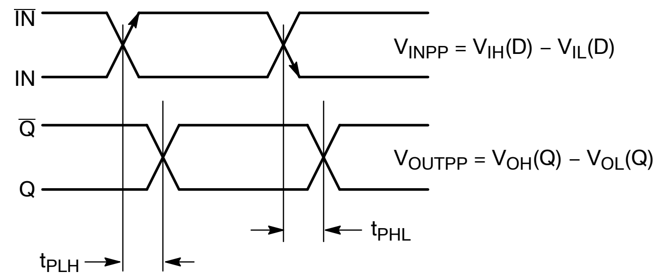



**Figure 5. AC Reference Measurement**

## Cascading Multiple EP195s

To increase the programmable range of the EP195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple programmable delay chips will result in a larger programmable range: however, this increase is at the expense of a longer minimum delay.

Figure 6 illustrates the interconnect scheme for cascading two EP195s. As can be seen, this scheme can easily be expanded for larger EP195 chains. The D10 input of the EP195 is the CASCADE control pin. With the interconnect scheme of Figure 6 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device and switches output pin CASCADE HIGH and pin $\overline{\text{CASCADE}}$ LOW. The A11 address can be added to generate a cascade output for the next EP195. For a 2−device configuration, A11 is not required.

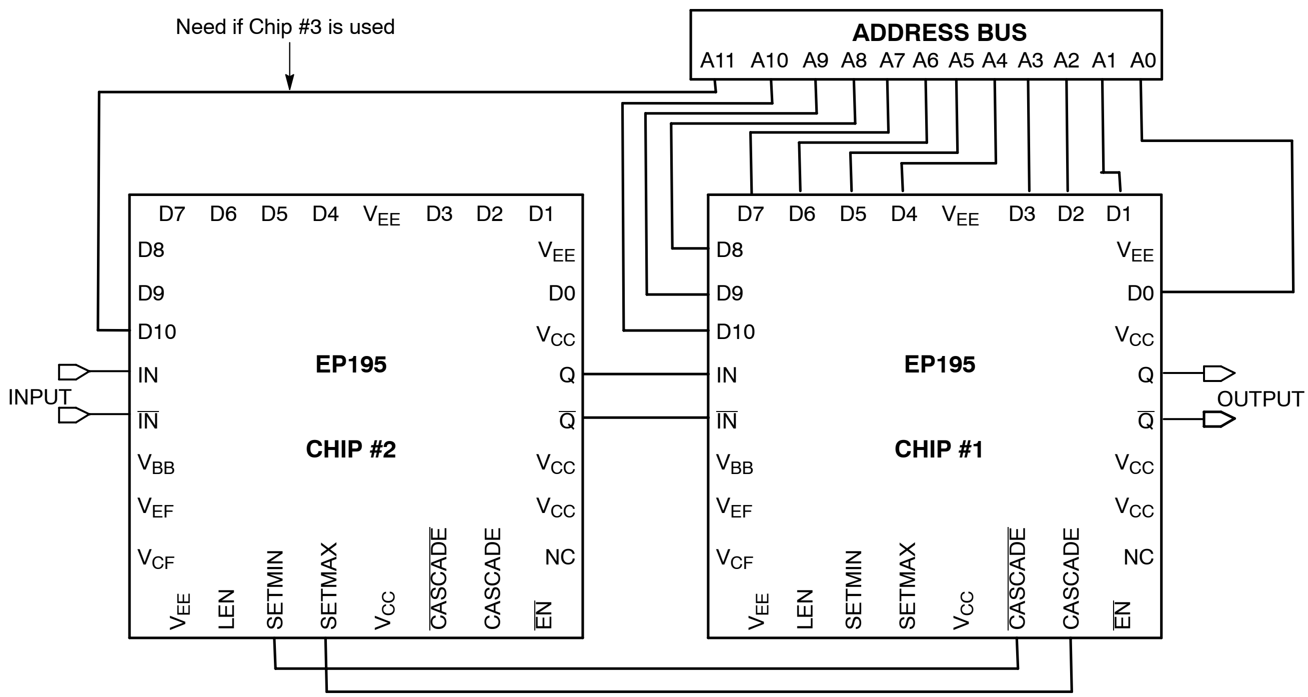



**Figure 6. Cascading Interconnect Architecture**

An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 6 is LOW this device's CASCADE output will also be low while the $\overline{\text{CASCADE}}$ output will be high. In this condition the SET MIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0—A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0—A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP195 device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 13 shows the delay time of two EP195 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

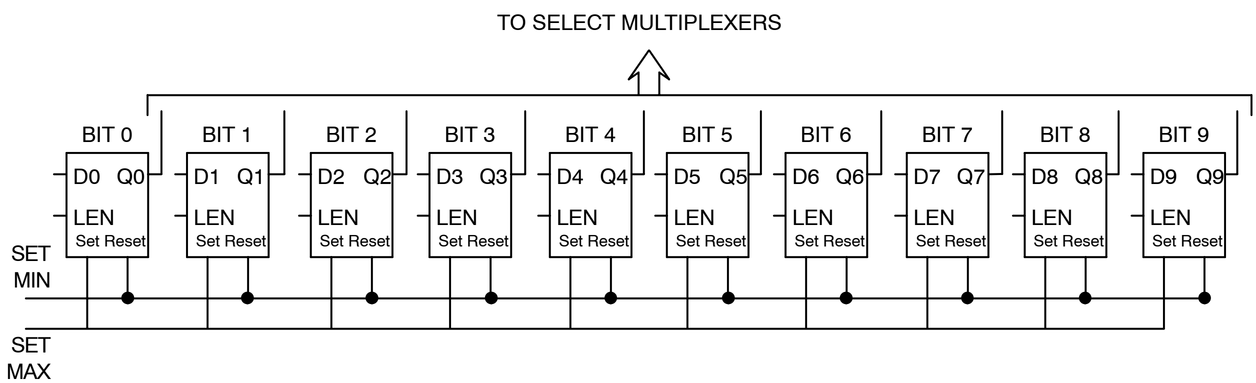



**Figure 7. Expansion of the Latch Section of the EP195 Block Diagram**

**Table 13. Delay Value of Two EP195 Cascaded**

| VARIABLE INPUT TO CHIP #1 AND *SETMIN* FOR CHIP #2 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INPUT FOR CHIP #1 | | | | | | | | | | | | Total |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Delay Value | Delay Value |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 ps | 4400 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 ps | 4410 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 20 ps | 4420 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 30 ps | 4430 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 40 ps | 4440 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 50 ps | 4450 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 60 ps | 4460 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 70 ps | 4470 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 80 ps | 4480 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 160 ps | 4560 ps |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 220 ps | 4720 ps |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 640 ps | 5040 ps |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1280 ps | 5680 ps |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2560 ps | 6960 ps |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5120 ps | 9520 ps |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 10230 ps | 14630 ps |

| VARIABLE INPUT TO CHIP #1 AND *SETMAX* FOR CHIP #2 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INPUT FOR CHIP #1 | | | | | | | | | | | | Total |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Delay Value | Delay Value |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10240 ps | 14640 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10250 ps | 14650 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 10260 ps | 14660 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 10270 ps | 14670 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 10280 ps | 14680 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10290 ps | 14690 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 10300 ps | 14700 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 10310 ps | 14710 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10320 ps | 14720 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10400 ps | 14800 ps |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10560 ps | 14960 ps |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 10880 ps | 15280 ps |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11520 ps | 15920 ps |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 12800 ps | 17200 ps |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 15360 ps | 19760 ps |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 20470 ps | 24870 ps |

### Multi−Channel Deskewing

The most practical application for EP195 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high−speed system. To deskew multiple signal channels, each channel can be sent through each EP195 as shown in Figure 8. One signal channel can be used as reference and the other EP195s can be used to adjust the delay to eliminate the timing skews. Nearly any high−speed system can be fine−tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.

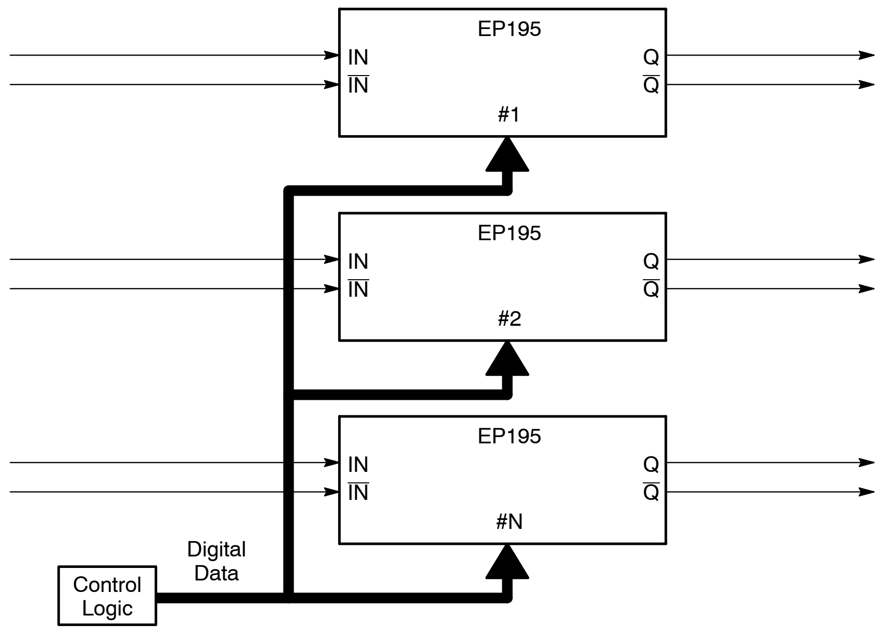



**Figure 8. Multiple Channel Deskewing Diagram**

### Measure Unknown High Speed Device Delays

EP195s provide a possible solution to measure the unknown delay of a device with a high degree of precision. By combining two EP195s and EP31 as shown in Figure 9, the delay can be measured. The first EP195 can be set to SETMIN and its output is used to drive the unknown delay device, which in turn drives the input of a D flip−flop of EP31. The second EP195 is triggered along with the first EP195 and its output provides a clock signal for EP31. The programmed delay of the second EP195 is varied to detect the output edge from the unknown delay device.

If the programmed delay through the second EP195 is too long, the flip−flop output will be at logic high. On the other hand, if the programmed delay through the second EP195 is too short, the flip−flop output will be at a logic low. If the programmed delay is correctly fine−tuned in the second EP195, the flip−flop will bounce between logic high and logic low. The digital code in the second EP195 can be directly correlated into an accurate device delay.

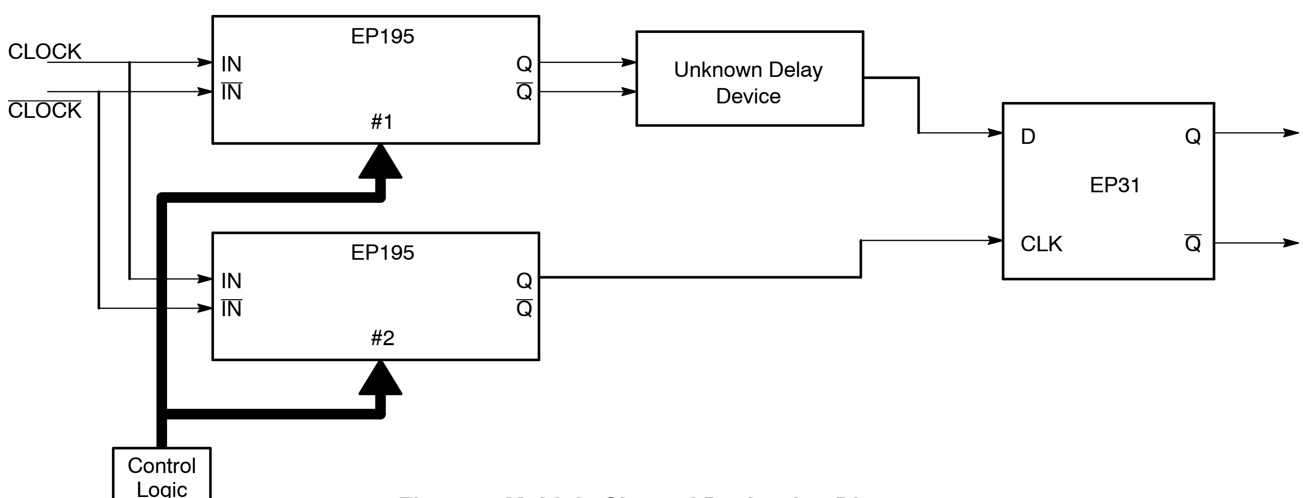



**Figure 9. Multiple Channel Deskewing Diagram**

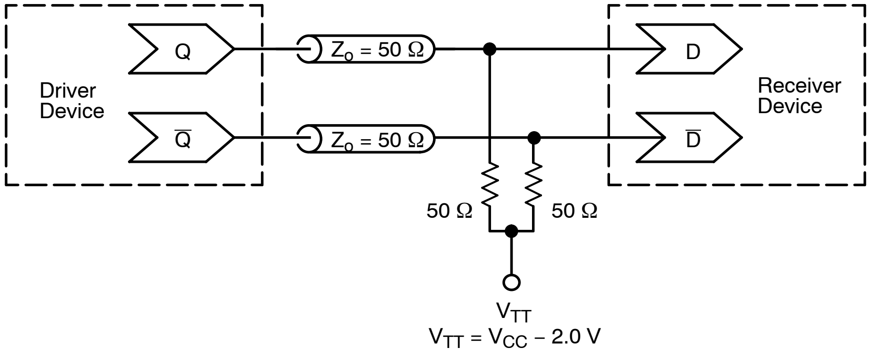



**Figure 10. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC10EP195FA | LQFP−32 | 250 Units / Tray |
| MC10EP195FAG | LQFP−32 (Pb−Free) | 250 Units / Tray |
| MC10EP195FAR2 | LQFP−32 | 2000 / Tape & Reel |
| MC10EP195FAR2G | LQFP−32 (Pb−Free) | 2000 / Tape & Reel |
| MC10EP195MNG | QFN−32 (Pb−Free) | 74 Units / Rail |
| MC10EP195MNR4G | QFN−32 (Pb−Free) | 1000 / Tape & Reel |
| MC100EP195FA | LQFP−32 | 250 Units / Tray |
| MC100EP195FAG | LQFP−32 (Pb−Free) | 250 Units / Tray |
| MC100EP195FAR2 | LQFP−32 | 2000 / Tape & Reel |
| MC100EP195FAR2G | LQFP−32 (Pb−Free) | 2000 / Tape & Reel |
| MC100EP195MNG | QFN−32 (Pb−Free) | 74 Units / Rail |
| MC100EP195MNR4G | QFN−32 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

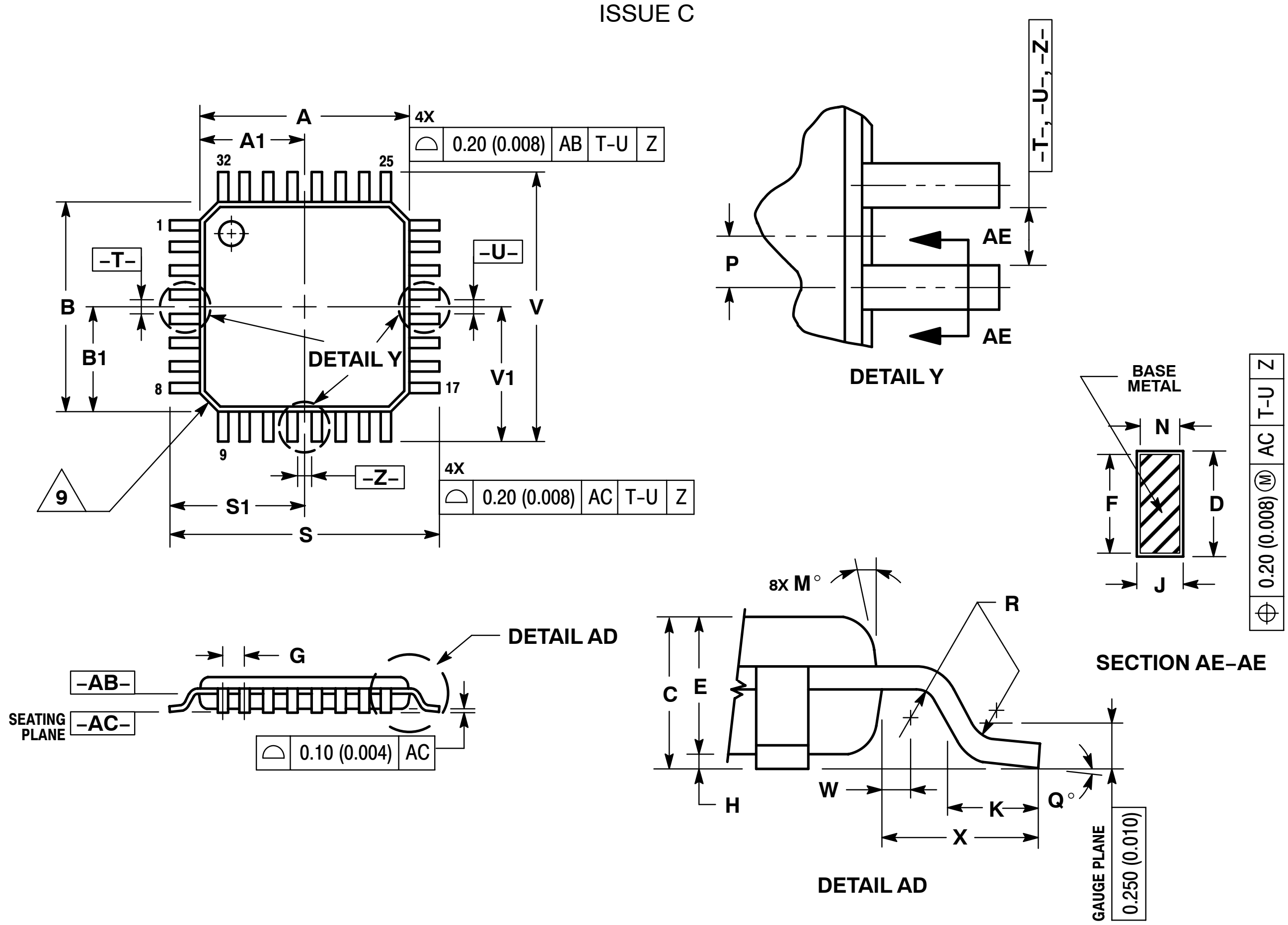
**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**32 LEAD LQFP**
CASE 873A−02
ISSUE C

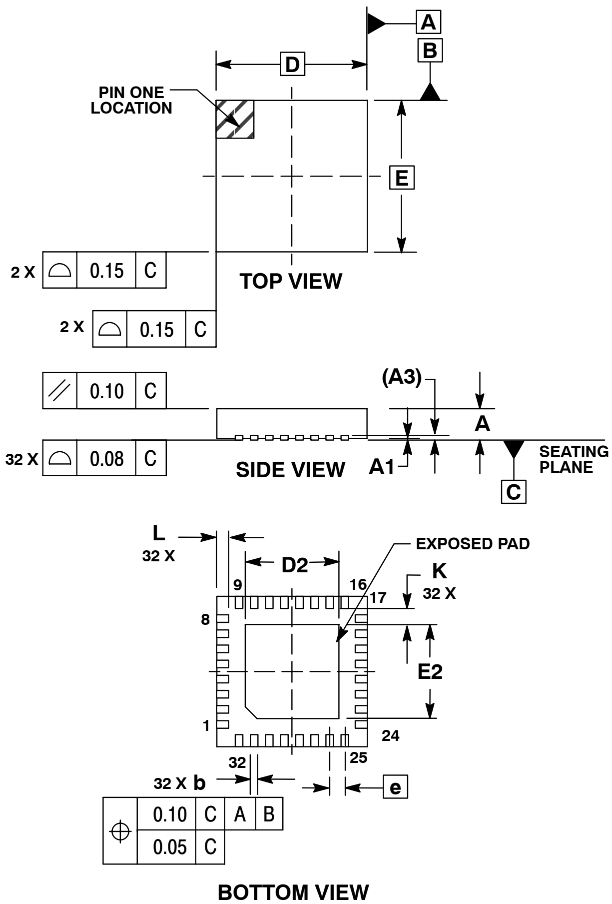



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.450 | 0.750 | 0.018 | 0.030 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

## PACKAGE DIMENSIONS

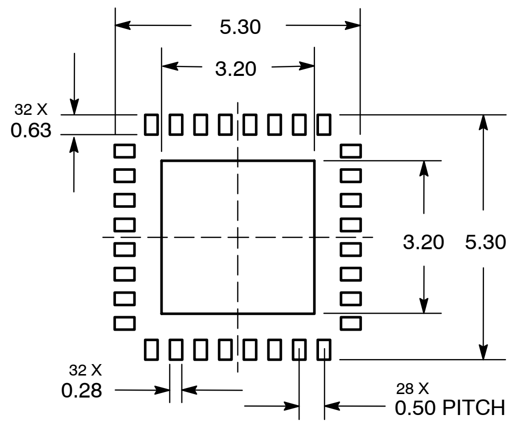
**QFN32 5*5*1 0.5 P**
CASE 488AM−01
ISSUE O




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | 0.200 REF | | |
| b | 0.180 | 0.250 | 0.300 |
| D | 5.00 BSC | | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | 5.00 BSC | | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | 0.500 BSC | | |
| K | 0.200 | --- | --- |
| L | 0.300 | 0.400 | 0.500 |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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